ABSTRACT OF THE DISCLOSURE

A low power, high performance flip-flop is disclosed. The novel flip-flop uses only one clocked transistor, whereas most traditional designs use three clocked transistors. The single clocked transistor is shared by the first and second branches of the device. A pulse generator produces a clock pulse to trigger the flip-flop. In one preferred embodiment the device can be made as a static explicit pulsed flip-flop which employs only two clocked transistors.